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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Divakaruni, et al

Serial No.: 09/718,850 Group Art Unit: 2811

Filed: November 22, 2000 Examiner: G. Munson

For: LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

Assistant Commissioner of Patents
Washington, D.C. 20231

SUBMISSION OF FORMAL DRAWINGS

Sir:

Submitted herewith are twelve (12) sheets of formal drawings comprising Figs. 1-20B for the above-referenced patent application. Acknowledgment of receipt is respectfully requested.

Please substitute these formal drawings for the drawings which were filed with the application.

Respectfully Submitted,

Frederick W. Gibb, III
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Date: 01/15/02

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): **Divakaruni et al.**			Docket No. **BUR920000016US1**
Serial No. **09/718,850**	Filing Date **November 22, 2000**	Examiner **G. Munson**	Group Art Unit **2811**

Invention: **LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR**

I hereby certify that this **SUBMISSION OF FORMAL DRAWINGS w/Figs. 1-20B**
(Identify type of correspondence)

is being deposited with the United States Postal Service as first class mail in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on January 15, 2002
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